

1 Amendments to the Claims:

2 This listing of claims will replace all prior versions, and
3 listings, of claims in the application using (Original) (Currently
4 Amended) (New) (Canceled) nomenclature, as recited in the below
5 listing of claims.

6 1. (Currently Amended) A timing recovery loop for generating
7 adjusted timing pulses from a baseband signal waveform encoding a
8 self clocking digital bit stream, the timing recovery loop
9 comprising,

10 a pulse detector for generating data transition pulses from the
11 baseband signal waveform, the pulse detector for comparing the data
12 transition pulses with the adjusted timing pulses for generating
13 early signals and lag signals, the data transition pulses
14 corresponding to respective data bits of the self clocking digital
15 bit stream with each of the data bits having a bit period, the data
16 transition pulses being synchronized to the baseband waveform,

17 a random walk counter for counting the early signals and lag
18 signals over a plurality of bit periods for generating a running
19 count, the early signals and lags signals being generated when the
20 data transistion pulses lead and lag the adjusted timing pulses,

21 a threshold comparator for determining when the running count
22 exceeds a predetermined first threshold count value, and

23 a timing pulse delay adjustor for adjusting an adjusted timing
24 pulse delay communicated to the pulse detector for delaying the
25 adjusted timing pulses for synchronizing the adjusted timing pulses
26 with the data transition pulses and with the baseband signal over a
27 plurality of bit periods when the running count exceeds the
28 predetermined threshold count value.

1 2. (Original) The timing recovery loop of claim 1 further
2 comprising,

3 a data detector for generating a reconstructed digital bit
4 stream by sampling the baseband signal waveform by the adjusted
5 timing pulses.

6

7 3. (Currently Amended) The timing recovery loop of claim 1 further
8 comprising,

9 a threshold count value selector for selecting the first
10 threshold count value.

11

12 4. (Currently Amended) The timing recovery loop of claim 1 further
13 comprising,

14 a threshold count value selector for selecting the first
15 threshold count value, and

16 an adaptive means for monitoring the rate at which the timing
17 pulse delay is adjusted, the threshold value count selector
18 adaptively selecting different first threshold count values when
19 the adjustment rate exceeds a predetermined rate being a second
20 threshold count value.

21

22

23

24

25

26

27

28 ///

1 5. (Currently Amended) The timing recovery loop of claim 1 further
2 comprising,

3 a count magnitude generator for generating the magnitude count
4 from the running count, the magnitude count being fed to the
5 threshold count comparator for determining when the running count
6 exceeds the predetermined first threshold count value, and

7 a count sign clipper for generating a count sign from the
8 running count, the count sign being fed to the timing pulse delay
9 adjustor for generating a timing pulse delay to adjust the adjusted
10 timing pulses, the sign count for increasing the timing pulse delay
11 when the data transition pulses arrive late relative to the
12 adjusted timing pulses and for decreasing the timing pulse delay
13 when the data transition pulses arrive early relative to the
14 adjusted timing pulses.

15
16
17
18 6. (Original) The timing recovery loop of claim 1 wherein the pulse
19 detector comprises,

20 a data transition pulse generator for generating the data
21 transition pulses,

22 a timing delay for delaying reference timing pulses into the
23 adjusted timing pulses, and

24 a lead and lag generator for generating lead and lag signals
25 for early and late arrivals of the data transition pulses relative
26 to the adjusted timing pulses.

27
28 ///

1 7. (Original) The timing recovery loop of claim 1 wherein the pulse
2 detector comprises,

3 a data transition pulse generator for generating the data
4 transition pulses,

5 a timing delay for delaying reference timing pulses into the
6 adjusted timing pulses, and

7 a data transition pulse counter for counting the number of
8 data transition pulses within a search window following an adjusted
9 timing pulse, and

10 a lead and lag generator for generating lead and lag signals
11 for early and late arrivals of the data transition pulses relative
12 to the adjusted timing pulses when one and only one data transition
13 pulse occurs within each search window following an adjusted timing
14 pulse.

15

16

17

18

19

20

21

22

23

24

25

26

27

28 ///

1 8. (Original) The timing recovery loop of claim 1 wherein the pulse
2 detector comprises,

3 a data transition pulse generator for generating the data
4 transition pulses,

5 a window delay for delaying the data transition pulses by half
6 of a search window to center the data transition pulses within
7 respective search windows,

8 a timing delay for delaying by a timing pulse delay the
9 reference timing pulses into the adjusted timing pulses, the timing
10 pulse delay being generated by the timing delay adjustor, the
11 timing pulse delay being adjusted when the running count exceeds
12 predetermined threshold value,

13 a data transition pulse counter for counting the number of
14 data transition pulses within the search window following an
15 adjusted timing pulse, and

16 a lead and lag generator for generating lead and lag signals
17 for early and late arrivals of the data transition pulses relative
18 to the adjusted timing pulses when one and only one data transition
19 pulse occurs within a respective one of the search windows
20 following a respective one of the adjusted timing pulses.

21
22 9. (Previously Presented) The timing recovery loop of claim 1,
23 wherein,

24 the random walk counter sums the lead signals and lag signals as
25 the running count.

26
27 ///
28
29